**Amendment to the Claims:**

This listing of claims replaces all prior versions and listings of claims in the application:

1. (Currently Amended) A method for controlling the access to all or part of the content of a ~~first~~ memory integrated with a microprocessor, the method comprising:

executing an access control algorithm contained in ~~a second~~ an auxiliary memory using a priority-holding interrupt (PRIORIN); and

accessing the content of the ~~first~~ memory with the access control algorithm using at least one register of keys,

wherein the ~~second~~ auxiliary memory is at least functionally distinct ~~and separate~~ from the ~~first~~ memory in that the memory is for containing embarked programs of a desired application and the auxiliary memory is not for containing the embarked programs of the desired application, and the content of the auxiliary memory being programmable only once.

2. (Currently Amended) The method of claim 1, wherein at least one sub-program authorizing the execution of a function of access to the ~~first~~ memory is contained in the auxiliary memory.

3. (Original) The method of claim 1, wherein the priority-holding interrupt (PRIORIN) is non-interruptible, even by itself.

4. (Original) The method of claim 1, wherein said priority-holding interrupt (PRIORIN) is generated provided that a signal (MODE) indicative of an access control operating mode is in an active state.

5. (Original) The method of claim 1, wherein said priority-holding interrupt (PRIORIN) can be generated upon occurrence of an interrupt request coming from the outside (EXTPRIORIN) of the integrated circuit or from the inside (INTPRIORIN).

6. (Canceled)

7. (Currently Amended) The method of claim ~~6~~ 1, wherein the accessing step ~~of accessing the content of the first memory with the access control algorithm using at least one register of keys~~ includes using the content of at least one integrated storage element along with the content of the key register.

8. (Currently Amended) A circuit comprising:

a microprocessor integrated with at least one ~~first~~ memory;

~~a second~~ an auxiliary memory containing at least one sub-program for accessing the content of the ~~first~~ memory, wherein said ~~second~~ auxiliary memory is at least functionally distinct ~~and separate~~ from the ~~first~~ memory in that the memory is for containing embarked programs of a desired application and the auxiliary memory is not for containing the embarked programs of the desired application, and the content of the auxiliary memory being programmable only once.

9. (Currently Amended) The circuit of claim 8, further including means for selecting, at an input of a memory interface of the microprocessor, a memory from among at least said auxiliary memory and said ~~first~~ memory, wherein

the selection of said ~~first~~ memory, otherwise that for the execution of ~~a function~~ one of the programs that it contains, requiring an authorization from an algorithm contained in the auxiliary memory and using the content of at least one integrated storage element and the content of ~~the~~ a key register.

10. (Currently Amended) The circuit of claim 9, wherein the ~~first~~ memory and the storage element are one and the same program memory.

11. (Currently Amended) The circuit of claim 8, further including means for generating a priority-holding interrupt for executing said sub-program, provided that:

a signal (MODE) indicative of an access-control operating mode is in an active state;

an access to the ~~first~~ memory has been requested otherwise than for a non-interruptible execution of one of the ~~functions~~ programs that it contains; and

an interrupt signal (EXTPRIORIN, INTPRIORIN) is active, wherein the resulting priority-holding interrupt being non-interruptible.

12. (Canceled)